PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Eric B. KUSHNICK

Art Unit: 2116

Application No: 09/824,898

Examiner:
Tse W. Chen

Filed: April 2, 2001

For: HIGH RESOLUTION CLOCK SIGNAL GENERATOR

TRANSMITTAL OF BRIEF ON BEHALF OF APPELLANT

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Notice of Appeal was filed in this case on May 12, 2006.

Submitted herewith in triplicate is Appellant's Brief.

A check in the amount of $500 for the fee under 37 CFR 41.20(b)(2) is enclosed.

Respectfully submitted,

Daniel J. Bedell
Reg. No. 30,156

SMITH-HILL & BEDELL, P.C.
16100 N.W. Cornell Road, Suite 220
Beaverton, Oregon 97006

Tel. (503) 574-3100
Fax (503) 574-3197
Docket: CRED 2164
Postcard: 05/06-15

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Penelope Stockwell

AF/2116

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Sir:

Real Party In Interest

Credence Systems Corporation

Related Appeals and Interferences

None

Status of Claims

Claims 1-14 and 17-38 are pending.

Claims 1-14 and 17-38 are rejected.

Claims 15 and 16 have been withdrawn.

Status of Amendments

An amendment after final rejection was filed to label FIG. 2 as "Prior Art". The amendment has not yet been entered.

Summary of Claimed Subject Matter

Claim 1

Claim 1 is best understood with reference to the applicant's FIG. 4. The invention as recited in claim 1 is an apparatus for generating

pulses of a third pulse sequence (CLOCK') in response to pulses of a periodic first pulse sequence (ROSC) having a period T_p. Claim 1 recites that the apparatus comprises

first means (54) for generating each pulse of a second pulse sequence (CLOCK) in response to a separate pulse of the first pulse sequence (ROSC) with a first delay adjustable by first control data (SW(A)) with a resolution of T_p/N over a first range substantially wider than T_p/M, wherein M and N are differing integers greater than one;

second means (56) for generating each pulse of the third pulse sequence (CLOCK') in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data (SW(B)) with a resolution of T_p/M over a second range substantially wider than T_p/N; and

a programmable sequencer (58) for changing a magnitude of the first control data (SW(A)) and the second control data (SW(B)) in response to each pulse of the first pulse sequence (ROSC) such that the magnitudes of the first and second control data vary repetitively in a programmable adjustable manner.

The invention can, for example, produce a periodic output signal (CLOCK') having a period that differs from that of a periodic input signal (ROSC) that it uses as a timing reference. We adjust the period of the CLOCK' signal by adjusting the repetitive first and second control data patterns produced by programmable sequencer 58.

Claim 3

Claim 3 depends on claim 1 and adds the limitation that "at least one of the first and second ranges is wider than T_p."

Claim 13

Claim 13, best understood with reference to the applicant's FIG. 7, adds the limitation that "the second means further comprises means (70) for monitoring a phase relationship between the first pulse sequence (ROSC) and the fourth pulse sequence (the unreferenced input to block 70) and adjusting the magnitude of the second control signal (CONTROL) so that the fourth pulse sequence is phase-clocked to the first pulse sequence."

Claim 17

Independent claim 17 has limitations similar to those of claim 1 but also recites some additional limitations with respect to the structure of the recited first and second means.

The "first means" can be implemented by the prior art block 24 of FIG. 1. Claim 17 recites that the "first means" (24) comprises a "plurality of first gates (16) connected in series for generating pulses of the second pulse sequence (CLOCK) in response to each pulse of the first pulse sequence (ROSC) … wherein each first gate has a switching delay of T_p/N."

The "second means" is best understood with reference to FIG. 7. Claim 17 recites that the "second means" (56) comprises

"a plurality of second gates (60) connected in series for generating pulses of the third pulse sequence (CLOCK') in response to pulses of the second pulse sequence (CLOCK)"; and

"M third gates (66) connected in series for generating a fourth pulse sequence (input to PLL controller 70) in delayed response to the first pulse sequence (ROSC)",

"wherein each second and third gate (60, 66) has a similar switching delay of T_p/M set by the magnitude of a third control signal (CONTROL(B)) applied to all of the second and third gates."

This particular architecture for the "second means" renders the switching delay (T_p/M) of each second gate a function only of the period T_p of a stable reference signal (ROSC) and to be independent of the period of the input signal (CLOCK) the second means delays. Thus the delay provided by the second state is a predictable function of its control data (SW)B) input and is not influenced by the period of the CLOCK signal being delayed.

Claim 13

Claim 13, best understood with reference to the applicant's FIG. 7, adds the limitation that "the second means further comprises means (70) for monitoring a phase relationship between the first pulse sequence (ROSC) and the fourth pulse sequence (the unreferenced input to block 70) and adjusting the magnitude of the second control signal

(CONTROL) so that the fourth pulse sequence is phase-clocked to the first pulse sequence."

Claim 20

Claim 20, best understood with reference to FIG. 4, is a method claim having limitations that are analogous to those of apparatus claim 1. Claim 20 recites a method for generating a third pulse sequence (CLOCK') in response to pulses of a periodic first pulse sequence (ROSC) having a period T_p. Claim 20 recites that the method comprises steps of

a. generating each pulse of a second pulse sequence (CLOCK) in response to a separate pulse of the first pulse sequence (ROSC) with a first delay adjustable by first control data (SW(A)) with a resolution of T_p/N over a first range substantially wider than T_p/M, wherein M and N are differing integers greater than one;

b. generating each pulse of the third pulse sequence (CLOCK') in response to a separate pulse of the second pulse sequence (CLOCK) with a delay adjustable by a second control data (SW(B)) with a resolution of T_p/M over a second range substantially wider than T_p/N; and

c. changing a magnitude of the first control data (SW(A)) and the second control data (SW(B)) in response to each pulse of the first pulse sequence (ROSC) such that the magnitudes of the first and second control data vary repetitively in a programmable adjustable manner.

Claim 34

Claim 34 is best understood with reference to FIG. 4. Claim 34 recites a method for generating a third pulse sequence (CLOCK') in response to pulses of a periodic first pulse sequence (ROSC) having a period T_p, the method comprising the steps of:

a. generating each pulse of a second pulse sequence (CLOCK) in response to a separate pulse of the first pulse sequence (ROSC) with a delay adjustable by first control data (SW(A)) with a resolution of T_p/N; and

b. generating each pulse of the third pulse sequence (CLOCK') in response to a separate pulse of the second pulse sequence (CLOCK) with a delay adjustable by a second control data (SW(B)) with a resolution of T_p/M; and

c. changing a magnitude of the first control data (SW(A)) and the second control data (SW(B)) in response to each pulse of the first pulse sequence (ROSC) such that the magnitudes of the first and second control data vary repetitively in a programmable adjustable manner, where M and N are relatively prime integers greater than one.

With M and N relatively prime, we can adjust the repetitive control data patterns produced by programmable sequencer 58 to adjust the period of the output signal (CLOCK') with a resolution that is higher than the delay resolution T_p/M or T_p/N of either the first or second means.

Grounds For Rejection To Be Reviewed On Appeal

Grounds for rejection to be reviewed on appeal are:

1. whether claims 1-2, 4-8, 11, 20-21, 23-27, 30, 34-35 should be rejected under 35 U.S.C. 102(b) as being anticipated by the manual "TTCrx Reference Manual" dated July 1997 by Christiansen et al, ("Christiansen");

2. whether claims 3 and 22 should be rejected under 35 U.S.C. 103(a) as being unpatentable over Christiansen in view of U.S. patent 6,194,92 issued to Heyne ("Heyne"); and

3. whether claims 9-10, 12-14, 17-19, 28, 29, 31-33, and 36-39 should be rejected under 35 U.S.C. 103(a) as being unpatentable over Christiansen in view of U.S. patent 6,388,485, issued May 14, 2002 to Kim ("Kim").

Arguments

1. Arguments against rejection of claims 1-2, 4-8, 11, 20-21, 23-27, 30, 34-35 under 35 U.S.C. 102(e) as being anticipated by Christiansen.

Claims 1, 2-4, and 11

Christiansen's FIG. 10 (the reference lacks page numbers) shows a two stage delay circuit that delays an input clock signal (in) to produce an output clock signal (out) by providing an adjustable number of gates in the signal path between in input and output signals. Each gate of the first stage provides a delay of T/N and each gate of the second stage provides a delay of T/(N-1). A separate multiplexer in

each stage selects the number of gates the stage places in the signal path.

The Examiner correctly points out at paragraph 6 (page 3) of the Office Action dated 2/14/2006 that the applicant's "first means" and "second means" of claim 1 read on the delay circuit of Christiansen's FIG. 10. However Christiansen fails to teach the "programmable sequencer" recited in claim 1 that changes the magnitude of the control data (sel) "in response to each pulse of the first pulse sequence [i.e. Christiansen's "in" signal) such that the magnitudes of the first and second control data vary repetitively in a programmably adjustable manner."

Christiansen's FIG. 10 does not show what provides the control data (sel) to the delay circuit of FIG. 10, but Christiansen's FIG. 4 depicts the context in which the delay circuit of FIG. 10 is used and the text preceding and following FIG. 4 discusses the nature and source of the control data. Christiansen's circuit of FIG. 4 is a receiver that produces a pair of clock signals CLK01 and CLK02 of phase and frequency controlled by a remote transmitter. The receiver of FIG. 4 receives data arriving via a digital signal ("input from PINFET"). The "clock extraction" circuit of FIG. 4 monitors the input signal to determine the frequency of the clock signal used to clock data onto the input signal and produces several output clock signals of that frequency. Some of the clock signals are provided to control timing in a "data decoder/demultiplexer" circuit which decodes the commands arriving on two data channels (A and B)of the input signal. The clock extraction circuit also supplies another clock signal to a pair of 'programmable fine deskew" circuits, each of which delays that clock signal by a separate amount to produce a separate one of output clock signals CLK01 and CLK02. Christiansen's FIG. 10 is provided as an example of either one of the two programmable fine deskew circuits of FIG. 4. Christiansen indicates (in the paragraph immediately above FIG. 4) that the data for controlling the deskew circuits arrives as commands on the B channel of the input signal. As discussed in the section following FIG. 4, that control data is loaded into Coarse Delay and Fine Delay registers of the "control & interface" block of FIG. 4 that provide the data as input to the programmable fine deskew circuits for controlling their delays. Presumably, this is the

control data (sel) that controls the delay through the first and second stages of the delay circuit of FIG. 10.

The remote transmitter apparently controls the frequency of the output clock signals CLK01 and CLK02 of the receiver circuit of FIG. 4 by setting the frequency of the clock signal it uses to clock data into the "input from PINFET" signal, and controls the phase of each of the CLK01 and CLK02 signal by sending commands over the B channel to set the delays of the fine deskew circuits. Christiansen teaches to use commands arriving by the B channel to set the deskew delay "to compensate for the time necessary to transmit and decode … commands". (See the section "Coarse Delay" under Christiansen's heading "TTCrx internal registers"). Thus it appears Christiansen's deskew circuits are used to compensate for the inherent transmission and processing delays in the path between the transmitter and receiver so that the CLK01 and CLK02 signals are of a desired phase. Christiansen provides no suggestion that whatever may be setting the value of delays control data would vary that control data "repetitively in a programmably adjustable manner" as recited in claim 1. Once the delays are set to properly compensate for the inherent delay of the signal path, there would be no reason to change the control data in the absence of any change to the signal path that would alter the path delay.

In any case, it would not be obvious for one of skill in the art to consider varying the delay control data inputs to the deskew circuits in a repetitive manner since doing so would render Christiansen's deskew circuits unfit for its intended purpose, which is to provide compensation for inherent signal path delays which do not vary in a repetitive manner.

The Examiner incorrectly argues at paragraph 6 (page 3) of the Office Action dated 2/14/2006 that the applicant's "programmable sequencer" reads on Christiansen's "programmable fine deskew" circuit of FIG. 4. The "programmable fine deskew circuit of FIG. 4 does not control the delay circuit of FIG. 10; it is the delay circuit of FIG. 10. Neither of the programmable deskew circuits of FIG. 4 can be considered a "programmable sequencer" for generating control data for any purpose. Their purpose is only to delay a clock signal. As discussed above, the control data for the delay/deskew circuits arrives by commands from a remote transmitter via the B channel of

the input signal, and Christiansen provides no suggestion that the remote transmitter might vary that control data in a repetitive manner as recited in claim 1.

At paragraph 45 of the same office action, the Examiner is apparently the opinion that the Applicant's observation that data supplied via channels A and B of the input signal of FIG. 4 controls the delay of the fine deskew circuits constitutes an admission that whatever supplies that data must be a "programmable sequencer" as recited in claim 1. However, as discussed above, Christiansen teaches that whatever in the transmitter controls the data transmitted on the A and B channels of the input signal sets the delay control data to compensate for inherent delays in the signal transmission and data processing path. Since there is no suggestion in Christiansen's teaching that such inherent delays vary in a repetitive manner, one of skill in the art would not be motivated to conclude that there is a programmable sequencer in the transmitter that varies the control data in some repetitive fashion.

It is also helpful to note that one of skill in the art would in any case not be motivated to vary the control data (sel) of Christiansen's delay circuit of FIG. 10 in response to each pulse of its input pulse sequence "in" because doing so could render Christiansen's delay circuit unstable. The Examiner (paragraph 46 of the office action dated 12/14/06) dismisses the applicant's explanation as to why Christiansen's circuit could become unstable if operated in this manner, saying

"Examiner was not able to find any explicit evidence in Christiansen's disclosure that supports the Applicant's hypothetical conclusion."

Thus the Examiner apparently reasons that if a cited reference does not explicitly teach that a circuit it describes could become unstable if controlled in some manner that the reference itself does not contemplate, then the Applicant's arguments to the contrary need not be considered. This is not a reasonable ground for rejecting the applicant's "hypothetical conclusion". In any case, the applicant's conclusion that Christiansen's circuit may become unstable if the "sel" data varies repetitively is not hypothetical, but is based on the following analysis of Christiansen's delay circuit of FIG. 10.

Note that the unit delay of each of the N+1 gates of Christiansen's second stage is T/(N+1), where T is the period of both the "in" signal and the output signal of the first stage multiplexer. A phase lock loop (PLL) circuit (the phase detector and loop filter) sets the delay of each of the N+1 gates to bring the periodic output signal of the last gate into phase with the periodic input signal of the first gate, thereby ensuring that each of those N+1 gates has a unit delay of T/(N+1), assuming the gates all have identical delays.

A feedback system such a Christianson's second stage PLL circuit needs a stable reference signal with which to compare the signal it controls. If its reference signal varies, the feedback system can become unstable as it tries to make the controlled signal match a moving target. The output signal of the multiplexer of the first stage of Christiansen's delay circuit of FIG. 10 is the reference signal for the second stage PLL circuit, which tries to make the phase of each edge of the output signal of the last gate of the N+1 gate series match the phase of each edge of the input signal of the first gate of the N+1 gate series. If a "programmable sequencer" were to constantly vary the "sel" control data input to the first stage multiplexer in a repetitive manner as recited in claim 1, then the phases of edges of the input signal to Christiansen's second stage could vary, and that could cause the PLL of the second stage to become unstable as it tries to match the phases of edges of the output signal of the last gate of the stage match to the changing phases of edges of the input signal to the first gate. Even if it doesn't become unstable, the second stage PLL would not be able to hold the unit delay of each of the N+1 gate to a constant value when the phase of the second stage input signal edges keeps changing. Thus the delay provided by Christiansen's delay circuit at any given moment would be unpredictable.

Though not recited as a limitation of claim 1, it is helpful to note that the applicant's two-stage delay circuit of the applicant's FIG. 5 overcomes this instability problem by making the unit delay of the gates 66 of the second stage (FIG. 7) independent of the period of the output signal (CLOCK) of the first stage. The PLL circuit of the second stage uses the ROSC signal (which has a constant phase and frequency) as a phase reference rather than the CLOCK signal output of

the first delay stage which may not be of constant phase and frequency when the control data input to the first stage constantly varies as recited in claim 1.

Thus Christiansen does not teach the programmable sequencer recited in claim 1, and one of skill in the art would not be motivated to use a programmable sequencer to vary the sel data in response to each pulse of the "in" of Christiansen's FIG. 10, because Christiansen doesn't suggest doing so, because doing so would render Christiansen's deskew circuit unfit for its intended purpose (deskewing) within the context of Christensen's application, and because doing so could render the Christiansen's delay circuit unstable or unpredictable. In order to avoid such problems, it would be necessary to modify Christiansen's circuit in some way not suggested by Christiansen.

Thus the rejection of claim 1 under 35 U.S.C. 102(e) in view of Christiansen was clearly incorrect and should be withdrawn. Claims 2-4 and 11 depend on claim 1 and are patentable over Christiansen for similar reasons.

Claims 20, 21, 23-27, 30, 34 and 35

Claims 20 and 34 recite a step c of

"changing a magnitude of the first control data and the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary repetitively in a programmable adjustable manner."
This is the function of the 'programmable sequencer of claim 1.

Claims 20 and 34 are therefore patentable over Christiansen for reasons similar to those discussed above in connection with claim 1. Claims 21, 23-27, 30, 34 and 35 are patentable over Christiansen for similar reasons.

2. Arguments against rejection of claims 3 and 22 under 35 U.S.C. 103(a) as being unpatentable over Christiansen in view of Heyne.

Claims 3 and 22

The Examiner cites Christiansen as teaching the subject matter of the parent claim 1 of claim 3 and relies on Heyne as teaching the additional limitations of claim 3. As discussed above Christiansen fails to teach the programmable sequencer recited in claim 1. Since Heyne also fails to teach the recited programmable sequencer, claim 3 is patentable over the combination of Christiansen and Heyne.

Referring to the applicant's FIG. 5, the applicant's claim 3 further recites that the delay range of either the first or second means (34 or 38) is wider than the period T_p of the delay circuit input first sequence (ROSC). The Examiner points to Heyne's FIG. 1 showing a two stage delay circuit and to Heyne's abstract, col. 2, lines 4-47 as teaching that at least one of the ranges of first stage (gates I1 and mux1) and the range of the second stage (gates I2 and Mux2) is larger than the period of the input signal (IN). However Heyne does not teach that the ranges of the first and second stages of Heyne's delay circuit of FIG. 1 ought to have any relation to a period of the IN signal. Heyne does not even suggest that the IN signal is periodic. Heyne (col. 5, line 55 though col. 6, line 10) does teach that the unit gate delays and ranges of the first and second stages should be sized relative to the expected fluctuation in the delay time of the delay circuit itself due to temperature variations. Such ranges have no relation to a period, if any, of the IN signal. Claim 22 is patentable over Christiansen and Heyne for similar reasons.

3. Argument against rejection of claims 9-10, 12-14, 17-19, 28, 29, 31-33, and 36-39 under 35 U.S.C. 103(a) as being unpatentable over Christiansen in view of Kim.

Claims 9, 10, 12, 17, 28, 29 and 31

Claim 17 is patentable over Christiansen for reasons similar to those expressed above in connection with claim 1. Claim 17 also recites additional limitations of the second means of claim 1 (as illustrated in the applicant's FIG. 7) that Christiansen fails to meet. The Examiner cites Kim as meeting those additional limitations.

As recited in claim 17, and as illustrated in FIG. 7, the "second means" comprises

"a plurality of second gates (60) connected in series for generating pulses of the third pulse sequence (CLOCK') in response to pulses of the second pulse sequence (CLOCK)"; and

"M third gates (66) connected in series for generating a fourth pulse sequence (input to PLL controller 70) in delayed response to the first pulse sequence (ROSC)",

"wherein each second and third gate (60, 66) has a similar switching delay of T_p/M set by the magnitude of a third control signal (CONTROL(B)) applied to all of the second and third gates."

If we compare the applicant's "second means" of FIG. 7, to Christiansen's second stage delay circuit of FIG. 10, we see that the applicant's FIG. 7 is a bit more complicated. The applicant's second stage has two sequences of gates (62 and 68) whereas Christiansen's second stage has only one sequence of gates. The applicant's circuit provides one sequence of gates 62 to delay the first stage output signal to produce the second stage output signal, and provides the extra sequence of gate 68 as a part of the PLL circuit which produces the control signal CONTROL(B) for controlling the unit delay of the gates of both sequences. Christiansen's single second stage sequence of N-1 gates does double duty in that it not only delays the first stage output signal to produce the second stage output signal (out), it also acts as part of a PLL circuit to produce a control signal for controlling the delay of each of its gates.

In Christiansen's circuit, the unit delay of each of the N-1 gates of the second stage is a function of the period of the output signal of the first stage and the PLL circuit uses the period T of that signal a timing reference which setting the delay T/(N-1) of each gate. That is an acceptable thing to do when the data input to the first stage multiplexer is constant so that edges of the output signal of the first stage are of constant phase. However, as discussed above, if we were to vary the control data (sel) input to the first stage multiplexer in a repetitive pattern , the PLL loop in the second stage could become unstable and the delay provided by each gate of the second stage could vary in an unpredictable manner.

The applicant's second stage circuit of claim 17 resolves this stability problem by employing two gate sequences (62 and 68) rather than one. Sequence 68 is used in the PLL circuit which sets the delay of each gate in both sequences to Tp/M where Tp is the period of a stable reference signal ROSC. Thus even when phases of edges of the CLOCK signal input that is delayed by the second stage vary in some repetitive pattern, the PLL remains stable and the delay of each gate 60 sequence 62 remains at the fixed predictable value of Tp/M.

KIM teach a delay circuit having a single delay stage 344 for delaying an input signal ECLK to produce an output signal ECLK. A PLL controller 30 produces a control signal DCON1 that controls the delay of the second stage. In this circuit the same input signal (ECLK) that is delayed by the delay stage also acts as the timing reference for the PLL circuit 30. Thus if one were to use a PLL arrangement similar to that described by KIM in place of Christiansen's second stage PLL controller, Christiansen's circuit would still fail to meet the limitations of claim 9 which uses a pulse sequence (ROSC) as a PLL reference signal that differs from the pulse sequence (CLOCK) being delayed by the second stage. As discussed above, using a different signal as a timing reference allows the two stage delay circuit to operate in a stable and predictable manner even when the phases of first stage output pulses vary repetitively.

The applicant's claim 17 is therefore patentable over the combination of Christiansen and Kim. Claims 9, 10, 12, 17, 28, 29 and 31 are patentable over Christiansen and Kim for similar reasons.

Claims 13, 14, 18, 19, 32, 33, 36-38

Claim 13 is patentable over Christiansen and Kim for reasons similar to those expressed above in connection with claim 17 and because claim 13 recites additional limitations not taught by Christiansen and Kim. Referring to the applicant's FIG. 7, claim 13 further recites "the second means further comprises means (70) for monitoring a phase relationship between the first pulse sequence (ROSC) and the fourth pulse sequence (other input to PL controller 70) and adjusting the magnitude of the second control signal (CONTROL(B)) so that the fourth pulse sequence is phase-clocked to the first pulse sequence."

In Christiansen's circuit, the "fourth pulse sequence" (i.e., the input to the second stage phase detector) is phase locked to the "second pulse sequence" (i.e., the output of the first stage multiplexer) rather than to the "first pulse sequence (i.e., the "in" signal input to the first stage) as recited in claim 1. This constitutes an additional reason for holding claim 13 patentable over Christiansen and Kim.

Claims 14, 18, 19, 32, 33, 36-38 are patentable over Christiansen and Kim for similar reasons.

CLAIMS APPENDIX

1. An apparatus for generating pulses of a third pulse sequence in response to pulses of a periodic first pulse sequence having a period T_P, wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than period T_P, the apparatus comprising:

first means for generating each pulse of a second pulse sequence in response to a separate pulse of the first pulse sequence with a first delay adjustable by first control data with a resolution of T_P/N over a first range substantially wider than T_P/M, wherein M and N are differing integers greater than one;

second means for generating each pulse of the third pulse sequence in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data with a resolution of T_P/M over a second range substantially wider than T_P/N; and

a programmable sequencer for changing a magnitude of the first control data and a magnitude of the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary repetitively in a programmably adjustable manner.

2. The apparatus in accordance with claim 1 wherein M and N are relatively prime.

3. The apparatus in accordance with claim 1 wherein at least one of said first and second ranges is wider than T_P.

4. The apparatus in accordance with claim 1 wherein the first range is at least as wide as $(1 - 1/N)T_P$ and the second range is at least as wide as $(1 - 1/M)T_P$.

5. The apparatus in accordance with claim 4 wherein M and N are relatively prime.

6. The apparatus in accordance with claim 1 wherein the third pulse sequence is periodic.

7. The apparatus in accordance with claim 1

wherein the first means comprises a plurality of first gates connected in series for generating pulses of the second pulse sequence in response to pulses of the first pulse sequence,

wherein each first gate has a switching delay of T_P/N.

8. The apparatus in accordance with claim 1

wherein the second means comprises a plurality of second gates connected in series for generating pulses of the third pulse sequence in response to pulses of the second pulse sequence; and

wherein each second gate has a switching delay of T_p/M.

9. The apparatus in accordance with claim 8

wherein the second means further comprises M third gates connected in series for generating a fourth pulse sequence in delayed response to the first pulse sequence; and

wherein each second and third gate has a similar switching delay of T_p/M set by the magnitude of a second control signal applied to all of the second and third gates.

10. The apparatus in accordance with claim 9

wherein the second means further comprises means for monitoring a phase relationship between the first pulse sequence and the fourth pulse sequence and adjusting the magnitude of the second control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

11. The apparatus in accordance with claim 1

wherein the first means comprises a plurality of first gates connected in series for generating pulses of the second pulse sequence in response to pulses of the first pulse sequence;

wherein the second means comprises a plurality of second gates connected in series for generating pulses of the third pulse sequence in response to pulses of the second pulse sequence;

wherein each first gate has a switching delay of T_P/N; and

wherein each second gate has a switching delay of T_P/M.

12. The apparatus in accordance with claim 11

wherein the second means further comprises M third gates connected in series for generating a fourth pulse sequence in delayed response to the first pulse sequence; and

wherein each second and third gate has a similar switching delay of T_P/M set by the magnitude of a second control signal applied to all of the second and third gates.

13. The apparatus in accordance with claim 12 wherein the second means further comprises means for monitoring a phase relationship between the first pulse sequence and the fourth pulse sequence and adjusting the magnitude of the second control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

14. The apparatus in accordance with claim 13

wherein said plurality of first gates includes N first gates connected in series and delaying the first pulse sequence to produce a fifth pulse sequence;

wherein the switching delay of each of said first gates is controlled by a magnitude of the first control signal supplied as input thereto; and

wherein the first means further comprises means for monitoring the first pulse sequence and the fifth pulse sequence and for adjusting the magnitude of the first control signal so that the fifth pulse sequence is phase-locked to the first pulse sequence.

17. An apparatus for generating pulses of a third pulse sequence in response to pulses of a periodic first pulse sequence having a period T_P, wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than T_P, the apparatus comprising:

first means for generating each pulse of a second pulse sequence in response to a separate pulse of the first pulse sequence with a delay adjustable by first control data with a resolution of T_P/N;

second means for generating each pulse of the third pulse sequence in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data with a resolution of T_P/M;

a programmable sequencer for changing a magnitude of the first control data and a magnitude of the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary repetitively in a programmably adjustable manner,

wherein the first means comprises a plurality of first gates connected in series for generating pulses of the second pulse sequence in response to pulses of the first pulse sequence,

wherein the second means comprises a plurality of second gates connected in series for generating pulses of the third pulse sequence in response to pulses of the second pulse sequence,

wherein each first gate has a switching delay of T_P/N,

wherein each second gate has a switching delay of T_P/M,

wherein the second means further comprises M third gates connected in series for generating a fourth pulse sequence in delayed response to the first pulse sequence, and

wherein each second and third gate has a similar switching delay of T_P/M set by the magnitude of a second control signal applied to all of the second and third gates.

18. The apparatus in accordance with claim 17 wherein the second means further comprises means for monitoring the first pulse sequence and the fourth pulse sequence and adjusting the magnitude of the

second control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

19. The apparatus in accordance with claim 18

wherein said plurality of first gates comprises N first gates connected in series and delaying the first pulse sequence to produce a fifth pulse sequence;

wherein the switching delay of each of said first gates is controlled by a magnitude of a first control signal supplied as input thereto; and

wherein the first means further comprises means for monitoring a phase relationship between the first pulse sequence and the fifth pulse sequence and for adjusting the magnitude of the first control signal so that the fifth pulse sequence is phase-locked to the first pulse sequence.

20. A method for generating pulses of a third pulse sequence in response to pulses of a periodic first pulse sequence having a period T_P, wherein timing of each pulse of the third
pulse sequence is adjustable with a resolution that is smaller than a period T_P, the method comprising the steps of:

a. generating each pulse of a second pulse sequence in response to a separate pulse of the first pulse sequence with a first delay adjustable by first control data with a resolution of T_P/N over a first range substantially wider than T_P/M, wherein M and N are differing integers greater than one;

b. generating each pulse of the third pulse sequence in response to a separate pulse of the second pulse sequence with a delay

adjustable by a second control data with a resolution of T_P/M over a second range substantially wider than T_P/N; and

c. changing a magnitude of the first control data and the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary repetitively in a programmably adjustable manner.

21. The method in accordance with claim 20 wherein M and N are relatively prime.

22. The method in accordance with claim 20 wherein at least one of said first and second ranges is wider than T_P.

23. The method in accordance with claim 20 wherein the first and second ranges are each at least as wide as T_P.

24. The method in accordance with claim 23 wherein M and N are relatively prime.

25. The method in accordance with claim 20 wherein the third pulse sequence is periodic.

26. The method in accordance with claim 20

wherein step a comprises applying the first pulse sequence as input to a plurality of first gates connected in series so that the first gates generate pulses of the second pulse sequence; and

wherein each first gate has a switching delay of T_P/N.

27. The method in accordance with claim 20

wherein step b comprises applying the second pulse sequence as input to a plurality of second gates connected in series so that the second gates generate pulses of the third pulse sequence; and

wherein each second gate has a switching delay of T_P/M.

28. The method in accordance with claim 27

wherein step b comprises applying the first pulse sequence as input to M third gates connected in series so that the third gates generate pulses of a fourth pulse sequence in delayed response to the first pulse sequence; and

wherein each second and third gate has a similar switching delay of T_P/M set by a magnitude of a control signal applied to all of the second and third gates.

29. The method in accordance with claim 28 wherein step b comprises the substeps of:

b1. monitoring a phase relationship between the first pulse sequence and the fourth pulse sequence; and

b2. adjusting the magnitude of the control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

30. The method in accordance with claim 20

wherein step a comprises applying the first pulse sequence as input to a plurality of first gates connected in series so that the first gates generate pulses of the second pulse sequence;

wherein step b comprises applying the second pulse sequence as input to a plurality of second gates connected in series so that the second gates generate pulses of the third pulse sequence;

wherein each first gate has a switching delay of T_P/N; and

wherein each second gate has a switching delay of T_P/M.

31. The method in accordance with claim 30

wherein step b comprises applying the first pulse sequence as input to M third gates connected in series so that the third gates generate pulses of a fourth pulse sequence in delayed response to the first pulse sequence; and

wherein each second and third gate has a similar switching delay of T_P/M set by the magnitude of a second control signal applied to all of the second and third gates.

32. The method in accordance with claim 31 wherein step b comprises the substeps of:

b1. monitoring a phase relationship between the first pulse sequence and the fourth pulse sequence; and

b2. adjusting the magnitude of the second control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

33. The method in accordance with claim 32

wherein said plurality of first gates comprises N first gates connected in series and delaying the first pulse sequence to produce a fifth pulse sequence;

wherein the switching delay of each of said first gates is controlled by a magnitude of a first control signal supplied as input thereto; and

wherein step a comprises the substeps of:

a1. monitoring a phase relationship between the first pulse sequence and the fifth pulse sequence; and

a2. adjusting the magnitude of the first control signal so that the fifth pulse sequence is phase-locked to the first pulse sequence.

34. A method for generating pulses of a third pulse sequence in response to pulses of a periodic first pulse sequence having a period T_P, wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than T_P, the method comprising the steps of:

a. generating each pulse of a second pulse sequence in response to a separate pulse of the first pulse sequence with a delay adjustable by a first control data with a resolution of T_P/N;

b. generating each pulse of the third pulse sequence in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data with a resolution of T_P/M; and

c. changing a magnitude of the first control data and a magnitude of the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary repetitively in a programmably adjustable manner, wherein M and N are relatively prime integers greater than one.

35. The method in accordance with claim 34

wherein step a comprises applying the first pulse sequence as input to a plurality of first gates connected in series so that the first gates generate pulses of the second pulse sequence;

wherein step b comprises applying the second pulse sequence as input to a plurality of second gates connected in series so that the second gates generate pulses of the third pulse sequence;

wherein each first gate has a switching delay of T_P/N; and

wherein each second gate has a switching delay of T_P/M.

36. The method in accordance with claim 35

wherein step b comprises applying the first pulse sequence as input to M third gates connected in series so that the third gates generate pulses of a fourth pulse sequence in delayed response to the first pulse sequence; and

wherein each second and third gate has a similar switching delay of T_P/M set by the magnitude of a second control signal applied to all of the second and third gates.

37. The method in accordance with claim 36 wherein step b comprises the substeps of:

b1. monitoring a phase relationship between the first pulse sequence and the fourth pulse sequence; and

b2. adjusting the magnitude of the second control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

38. The method in accordance with claim 37

wherein said plurality of first gates comprises N first gates

connected in series and delaying the first pulse sequence to produce a fifth pulse sequence;

wherein the switching delay of each of said first gates is controlled by a magnitude of a first control signal supplied as input thereto; and

wherein step a comprises the substeps of:

a1. monitoring a phase relationship between the first pulse sequence and the fifth pulse sequence; and

a2. adjusting the magnitude of the first control signal so that the fifth pulse sequence is phase-locked to the first pulse sequence.

Respectfully submitted,

Daniel J. Bedell
Reg. No. 30,156

SMITH-HILL & BEDELL, P.C.
16100 N.W. Cornell Road, Suite 220
Beaverton, Oregon 97006

Tel. (503) 574-3100
Fax (503) 574-3197
Docket: CRED 2164
Postcard: 05/06-15

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Penelope Stockwell